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10/573,492	05/15/2006	Koichi Naniwae	80741143	9283

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EXAMINER	
JONES, ERIC W	

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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/573,492	NANIWAE, KOICHI	
	Examiner	Art Unit	
	ERIC W. JONES	2892	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *30 April 2008*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-38* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-38* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *24 March 2006* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date *3/24/2006 and 6/27/2006*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Election/Restrictions

1. Claims 39-48 are withdrawn from further consideration pursuant to 37 CFR 1.142(b) as being drawn to a nonelected device, there being no allowable generic or linking claim. Election was made **without** traverse in the reply filed on 4/30/2008.

2. Applicant's election without traverse of claims 1-38 in the reply filed on 4/30/2008 is acknowledged.

Drawings

3. The drawings are objected to under 37 CFR 1.83(a). The drawings must show every feature of the invention specified in the claims. Therefore, 'the causing an etching agent having an etching action with respect to the semiconductor layer and crystal growth source material to come into contact with the semiconductor layer' of claims 1-3 and 19-21 must be shown or the feature(s) canceled from the claim(s). No new matter should be entered.

Corrected drawing sheets in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. Any amended replacement drawing sheet should include all of the figures appearing on the immediate prior version of the sheet, even if only one figure is being amended. The figure or figure number of an amended drawing should not be labeled as "amended." If a drawing figure is to be canceled, the appropriate figure must be removed from the replacement sheet, and where necessary, the remaining figures must be renumbered and appropriate changes made to the brief description of the several views of the drawings for

consistency. Additional replacement sheets may be necessary to show the renumbering of the remaining figures. Each drawing sheet submitted after the filing date of an application must be labeled in the top margin as either "Replacement Sheet" or "New Sheet" pursuant to 37 CFR 1.121(d). If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

Claim Rejections - 35 USC § 102

4. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

5. Claims 1-3, 11-17, 19-21, 29-35 and 37 are rejected under 35 U.S.C. 102(b) as being anticipated by Goto et al (5,400,740).

Re claim 1, Goto et al disclose a cleaning treatment method for eliminating contaminant adhered to the surface of a semiconductor layer, comprising:

a cleaning treatment step of simultaneously causing an etching agent (hydrogen chloride, HCl) having an etching action with respect to the semiconductor layer (Si-doped GaAs) and crystal growth source material (trimethyl gallium, TMG and arsine, AsH_3) to come into contact with the semiconductor layer. (column 3, lines 60-68; column 4, lines 1-33)

Re claim 2, Goto et al disclose a cleaning treatment method for eliminating contaminant adhered to the surface of a semiconductor layer, comprising:

a cleaning treatment step of exposing the surface of the semiconductor layer to an atmosphere containing an etching agent (hydrogen chloride, HCl) having an etching action with respect to the semiconductor layer and crystal growth source material (trimethyl gallium, TMG and arsine, AsH_3). (column 3, lines 60-68; column 4, lines 1-33)

Re claim 3, Goto et al disclose a cleaning treatment method for eliminating contaminant adhered to the surface of a semiconductor layer, comprising:

a cleaning treatment step of simultaneously providing a first gas including an etching agent (hydrogen chloride, HCl) having an etching action with respect to the semiconductor layer (Si-doped GaAs) and a second gas including crystal growth source material (trimethyl gallium, TMG and arsine, AsH_3) to the surface of the semiconductor layer. (column 3, lines 60-68; column 4, lines 1-33)

Re claims 11 and 29, Goto et al disclose the crystal growth source material includes an element (gallium and arsenic) constituting the semiconductor layer (GaAs). (column 3, lines 60-68)

Re claims 12 and 30, Goto et al disclose the crystal growth source material includes organic metal (trimethyl gallium, TMG). (column 3, lines 60-63)

Re claims 13 and 31, Goto et al disclose the etching agent is a halogen compound (hydrogen chloride, HCl). (column 3, lines 64-65)

Re claims 14 and 32, Goto et al disclose the semiconductor layer is comprised of compound semiconductor (Si-doped GaAs). (column 3, lines 65-68)

Re claims 15 and 33, Goto et al disclose the semiconductor layer is comprised of a group III- V compound (Si-doped GaAs) semiconductor. (column 3, lines 65-68)

Re claims 16 and 34, Goto et al disclose the crystal growth source material is a compound (trimethyl gallium, TMG) including a group III element (gallium, Ga) constituting the semiconductor layer (Si-doped GaAs). (column 3, lines 60-68)

Re claims 17 and 35, Goto et al disclose the group III element (gallium, Ga) constituting the semiconductor layer (Si-doped GaAs) is comprised of a single species. (column 3, lines 60-63)

Re claim 19, Goto et al disclose a method of manufacturing a semiconductor device comprising the steps of:

forming a first semiconductor layer (1.5 μm Si-doped GaAs) at an upper part of a semiconductor substrate ([100] Si-doped GaAs); subjecting the surface of the first semiconductor layer to cleaning treatment (etching); and forming a second semiconductor layer (0.5 μm Si-doped GaAs) on the first semiconductor layer, wherein the step of subjecting the surface of the first semiconductor layer to cleaning treatment includes a step of causing an etching agent (hydrogen chloride, HCl) having an etching action with respect to the semiconductor layer and crystal growth source material (trimethyl gallium, TMG and arsine, AsH_3) to come into contact with the surface of the semiconductor layer. (column 3, lines 60-68; column 4, lines 1-33)

Re claim 20, Goto et al disclose a method of manufacturing a semiconductor device comprising the steps of:

forming a first semiconductor layer (1.5 μm Si-doped GaAs) at an upper part of a semiconductor substrate ([100] Si-doped GaAs); subjecting the surface of the first semiconductor layer to cleaning treatment (etching); and forming a second

semiconductor layer (0.5 μm Si-doped GaAs) on the first semiconductor layer, wherein the step of subjecting the surface of the first semiconductor layer to cleaning treatment includes a step of exposing the surface of the semiconductor layer to an atmosphere containing an etching agent (hydrogen chloride, HCl) having an etching action with respect to the semiconductor layer and crystal growth source material (trimethyl gallium, TMG and arsine, AsH_3). (column 3, lines 60-68; column 4, lines 1-33)

Re claim 21, Goto et al disclose a method of manufacturing a semiconductor device comprising the steps of:

forming a first semiconductor layer (1.5 μm Si-doped GaAs) at an upper part of a semiconductor substrate ([100] Si-doped GaAs); subjecting the surface of the first semiconductor layer to cleaning treatment (etching); and forming a second semiconductor layer (0.5 μm Si-doped GaAs) on the first semiconductor layer, wherein the step of subjecting the surface of the first semiconductor layer to cleaning treatment includes a step of simultaneously supplying a first gas including an etching agent (hydrogen chloride, HCl) having an etching action with respect to the semiconductor layer and a second gas including crystal growth source material (trimethyl gallium, TMG) to the surface of the semiconductor layer. (column 3, lines 60-68; column 4, lines 1-16)

Re claim 37, Goto et al disclose the first semiconductor layer (1.5 μm Si-doped GaAs) and the second semiconductor layer (0.5 μm Si-doped GaAs) are formed using vapor phase epitaxy (Metal-Organic Vapor Phase Epitaxy, MOVPE). (column 3, lines 60-68; column 4, lines 1-5)

Claim Rejections - 35 USC § 103

6. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

7. Claims 4, 18, 22 and 36 are rejected under 35 U.S.C. 103(a) as being unpatentable over Goto et al in view of Nakamura et al (5,785,755).

Re claims 4 and 22, Goto et al fail to disclose the first gas and the second gas are supplied in an intermittent manner.

Nakamura et al disclose vapor phase epitaxy using intermittent flows (FIG. 1) of trimethylindium (TMI), triethylgallium (TEG), PH3, and AsH_3. (column 2, lines 64-67)

It would have been obvious to one of ordinary skill in the art at the time the invention was made to substitute the vapor phase epitaxy using intermittent flows of Nakamura et al for the gas flow method of Goto et al to provide a multilayer crystal film of InGaAsP, where the layers have different group V element compositions. (column 1, lines 48-51)

Re claims 18 and 36, Goto et al fail to disclose the group III element constituting the semiconductor layer is indium (In).

Nakamura et al disclose vapor phase epitaxy using intermittent flows (FIG. 1) of trimethylindium (TMI) for growth on an InGaAsP multiple quantum well (MQW) structure. (column 2, lines 64-67)

It would have been obvious to one of ordinary skill in the art at the time the invention was made to substitute the InGaAsP multiple quantum well (MQW) structure of Nakamura et al for the Si-doped semiconductor layers of Goto et al to provide a multilayer crystal film of InGaAsP, where the layers have different group V element compositions. (column 1, lines 48-51)

8. Claims 5-10 and 23-28 are rejected under 35 U.S.C. 103(a) as being unpatentable over Goto et al in view of Shimoyama et al (5,827,365).

Re claims 5 and 23, Goto et disclose etching 0.3 μm (3000 nm) of the Si-doped semiconductor layer. (column 4, lines 6-11)

Goto et al fail to disclose a difference in layer thickness of the semiconductor layer before and after implementation of the cleaning treatment step is 100 nm or less.

It would have been obvious to one of ordinary skill in the art at the time the invention was made to have a difference in layer thickness of the semiconductor layer before and after implementation of the cleaning treatment step is 100 nm or less, since it has been held that where the general conditions of a claim are disclosed in the prior art, discovering the optimum or workable ranges involves only routine skill in the art. *In re Aller*, 105 USPQ 233. See MPEP § 2144.05.

Re claims 6 and 24, Goto et disclose etching 0.3 μm (3000 nm) of the Si-doped semiconductor layer. (column 4, lines 6-11)

Goto et al fail to disclose layer thickness of the semiconductor layer is not substantially reduced during implementation of the cleaning treatment step.

It would have been obvious to one of ordinary skill in the art at the time the invention was made to have a layer thickness of the semiconductor layer that is not substantially reduced during implementation of the cleaning treatment step, since it has been held that where the general conditions of a claim are disclosed in the prior art, discovering the optimum or workable ranges involves only routine skill in the art. *In re Aller*, 105 USPQ 233. See MPEP § 2144.05.

Re claims 7 and 25, Goto et al disclose change in layer thickness (etching grade) of the semiconductor layer is controlled by adjusting the quantitative ratio of the etching agent (hydrogen chloride, HCl) and the crystal growth source material (trimethyl gallium, TMG and arsine, AsH_3). (column 4, lines 26-31)

Re claims 8-10 and 26-28, Goto et al fail to disclose a symbol for rate of change of layer thickness of the semiconductor layer is positive when layer thickness increases and is negative when layer thickness decreases; rate of change of layer thickness of the semiconductor layer during implementation of the cleaning treatment step is R; rate of change of layer thickness of the semiconductor layer in the case of supplying only the first gas to the semiconductor layer surface is r1, and rate of change of layer thickness of the semiconductor layer in the case of supplying only the second gas to the semiconductor layer surface is r2, the amount of the first gas and the second gas supplied is adjusted in such a manner that an absolute value for the rate of change of layer thickness becomes: $|R| < |r2| < |r1|$; wherein $R<0$; and $|R|$ is 0.1 nm/sec or less.

Shimoyama et al disclose the growth rate of a semiconductor layer (AlGaAs) decreases by 2% with the addition of HCl to growth gases trimethylgallium (TMG), trimethylaluminum (TMA) and arsine (AsH_3). (column 4, lines 25-47)

It would have been obvious to one of ordinary skill in the art at the time the invention was made that flowing only the growth gases results in a higher rate of change of layer thickness than the rate of change of layer thickness due to flowing HCl alone, since the HCl has an etching effect on the layer.

Also, it would have been obvious to one of ordinary skill in the art at the time the invention was made to have a symbol for rate of change of layer thickness of the semiconductor layer is positive when layer thickness increases and is negative when layer thickness decreases; rate of change of layer thickness of the semiconductor layer during implementation of the cleaning treatment step is R; rate of change of layer thickness of the semiconductor layer in the case of supplying only the first gas to the semiconductor layer surface is r1, and rate of change of layer thickness of the semiconductor layer in the case of supplying only the second gas to the semiconductor layer surface is r2, the amount of the first gas and the second gas supplied is adjusted in such a manner that an absolute value for the rate of change of layer thickness becomes: $|R| < |r2| < |r1|$; wherein $R<0$; and $|R|$ is 0.1 nm/sec or less, since it has been held that where the general conditions of a claim are disclosed in the prior art, discovering the optimum or workable ranges involves only routine skill in the art. *In re Aller*, 105 USPQ 233. See MPEP § 2144.05.

9. Claim 38 is rejected under 35 U.S.C. 103(a) as being unpatentable over Goto et al in view of Kimura et al (5,679,603).

Re claim 38, Goto et al fail to disclose a mask is formed on the first semiconductor layer after the step of forming the first semiconductor layer, and after eliminating the mask, the step of subjecting the surface of the first semiconductor layer to cleaning treatment is implemented.

Kimura et al disclose forming a mask (SiO2 stripe 50 in FIG. 11b) after forming a first semiconductor layer (InP 3 in FIG. 11a), and after eliminating the mask (FIG. 11d), the step of subjecting the surface of the first semiconductor layer to cleaning treatment (HCl etching) is implemented. (column 14, lines 20-41; column 15, lines 64-67; column 16, lines 1-5)

It would have been obvious to one of ordinary skill in the art at the time the invention was made to use the formation of a mask on the first semiconductor layer after the step of forming the first semiconductor layer, and after eliminating the mask, the step of subjecting the surface of the first semiconductor layer to cleaning treatment is implemented of Kimura et al with the method of Goto et al to provide a high resistance compound semiconductor layer which can suppress diffusion of impurities. (column 3, lines 1-10)

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to ERIC W. JONES whose telephone number is (571)270-3416. The examiner can normally be reached on Monday-Friday 5:30AM-3:00PM EST.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Thao X. Le can be reached on (571)272-1708. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

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8/21/2008